**IN THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) An inspecting circuit of a semiconductor device comprising:

at least first and second signal lines;

at least first, ~~and~~ second, and third NANDs, each of the first, ~~and~~ second, and third NANDs having first and second input terminals; and

an output terminal electrically connected to outputs of the first, ~~and~~ second, and third NANDs;

wherein an output of the first NAND is electrically connected to the first input terminal of the second NAND, ~~and~~

wherein an output of the second NAND is electrically connected to the first input terminal of the third NAND,

wherein the second input terminals of the first, ~~and~~ second, and third NANDs are ~~directly~~ connected to first, ~~and~~ second, and third signal lines, respectively, and

wherein a determination of whether the semiconductor device is normally operated or not is ~~performed by using~~ based on at least a signal obtained at the output terminal.

2. (Previously presented) The inspecting circuit of a semiconductor device according to claim 1, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

3. (Previously presented) The inspecting circuit of a semiconductor device according to claim 1, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line

through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

4. (Previously presented) The inspecting circuit of a semiconductor device according to claim 3, wherein an ExNOR is used for the comparator circuit.

5. (Currently amended) An inspecting circuit of a semiconductor device comprising;

at least first, ~~and~~ second, and third signal lines;

at least first ~~and~~ second, and third NANDs, each of the first, ~~and~~ second, and third NANDs having first and second input terminals; and

an output terminal electrically connected to outputs of the first, ~~and~~ second, and third NANDs,

wherein an output of the first NAND is electrically connected to the first input terminal of the second NAND, ~~and~~

wherein an output of the second NAND is electrically connected to the first input terminal of the third NAND,

wherein the second input terminals of the first, ~~and~~ second, and third NANDs are ~~directly~~ connected to first, ~~and~~ second, and third signal lines, respectively, and

wherein a determination of whether the semiconductor device is normally operated or not is ~~performed by~~ based on comparing an output pattern obtained at the output terminal and a reference pattern.

6. (Previously presented) The inspecting circuit of a semiconductor device according to claim 5, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of

the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

7. (Previously presented) The inspecting circuit of a semiconductor device according to claim 5, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

8. (Previously presented) The inspecting circuit of a semiconductor device according to claim 7, wherein an ExNOR is used for the comparator circuit.

9. (Currently amended) A semiconductor device comprising:

a source driver which inputs a clock signal, a start pulse and a video signal and outputs a plurality of signals to a plurality of source signal lines in accordance with the clock signal, the start pulse and the video signal;

an inspecting circuit including a plurality of input terminals and an output terminal at which an output of an inspection is obtained,

wherein the plurality of signals outputted to the plurality of source signals lines are inputted to the plurality of input terminals,

wherein a determination whether the semiconductor device is normally operated or not is ~~performed by~~ based on comparing an output pattern obtained at the output terminal and a reference pattern.

10. (Previously presented) The inspecting circuit of a semiconductor device according to claim 9, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

11. (Previously presented) The inspecting circuit of a semiconductor device according to claim 9, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

12. (Previously presented) The inspecting circuit of a semiconductor device according to claim 11, wherein an ExNOR is used for the comparator circuit.

13. (Currently amended) A semiconductor device comprising:

a gate driver which inputs a clock signal and a start pulse and sequentially outputs a select pulse to a plurality of gate signal lines in accordance with the clock signal and the start pulse;

an inspecting circuit including a plurality of latch circuits sampling a signal for inspection in

accordance with the select pulse, a plurality of input terminals to which output signals from the plurality of latch circuits are inputted, and an output terminal at which an output of an inspection is obtained,

wherein a determination whether the semiconductor device is normally operated or not is ~~performed by~~ based on comparing an output pattern obtained at the output terminal and a reference pattern.

14. (Previously presented) The inspecting circuit of a semiconductor device according to claim 13, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

15. (Previously presented) The inspecting circuit of a semiconductor device according to claim 13, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output

terminal at which an output of an inspection is obtained.

16. (Previously presented) The inspecting circuit of a semiconductor device according to claim 15, wherein an ExNOR is used for the comparator circuit.

17. (Previously presented) An inspecting circuit of a semiconductor device comprising:

a plurality of NANDs, a plurality of NORs, and a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal a NOR of i-th line (i is an integer number of two or more) in the plurality or NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

18. (Previously presented) An inspecting circuit of a semiconductor device comprising:

a plurality of NANDs, a plurality of NORs, a plurality of inverters, and a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal a NOR of i-th line (i is an integer number of two or more) in the plurality or NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to a first input terminal of the comparator circuit;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to a second input terminal of the comparator circuit; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

19. (Previously presented) The inspecting circuit of a semiconductor device according to claim 18, wherein an ExNOR is used for the comparator circuit.

20. (Previously presented) An inspecting method of a semiconductor device comprising the steps of:

simultaneously inputting a signal to each first input terminal of n NANDs included in an inspecting circuit, wherein an output of i-th NAND is inputted to a second input terminal of (i+1)th

NAND;

obtaining an output pattern from the inspecting circuit; and

determining an operation of the semiconductor device to be good or defective by comparing the output pattern and a reference pattern.

21. (Previously presented) An inspecting method of a semiconductor device, comprising the steps of:

sampling signals for inspection sequentially in accordance with signals outputted sequentially from a plurality of output signal lines;

simultaneously inputting each of the sampled signals to each first input terminal of n NANDs included in an inspecting circuit, wherein an output of i-th NAND is inputted to a second input terminal of (i+1)th NAND;

obtaining an output pattern from the inspecting circuit; and

determining an operation of the semiconductor device to be good or defective by comparing the output pattern and a reference pattern.

22. (New) A semiconductor device comprising:

a shift register; and

an inspecting circuit comprising:

at least first and second signal lines;

at least first and second NANDs, each of the first and second NANDs having first and second input terminals; and

an output terminal electrically connected to outputs of the first and second NANDs;

wherein an output of the first NAND is electrically connected to the first input terminal of the second NAND,

wherein the second input terminals of the first and second NANDs are connected to the first and second signal lines, respectively,

wherein the first and second signal lines are electrically connected to the shift register, and

wherein a determination whether the semiconductor device is normally operated or not is based on at least a signal obtained at the output terminal.

23. (New) The semiconductor device according to claim 22, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

24. (New) The semiconductor device according to claim 22, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically

connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

25. (New) The semiconductor device according to claim 22, wherein an ExNOR is used for the comparator circuit.